AMENDMENTS TO CLAIMS:

The listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (currently amended) A method comprising: ~~for high speed addressing of memory locations within the same page by accessing a first selected location in the memory space using at least a first and a second part of the address of the selected location, the method comprising the steps of:~~

determining that a first condition is true, the first condition being that an address of a first location in a memory space has been transmitted on a bus, the address of the first location including at least one first part and a second part;

~~(a)~~ determining that a second condition is true, the second condition being that at least one first part of an address of a second location in the memory space has been transmitted on the bus in a particular address cycle; ~~transmitting a first part of the address of a second selected location in the memory space~~;

determining that a third condition is true, the third condition being that a first control signal associated with the bus indicates that a next bus cycle following the particular address cycle is not an address cycle; and

~~(b)~~ determining, if the first, second, and third conditions are true, that the second part of the address of the first location is substantially equivalent to a second part of the address of the second location. ~~whether at least a second part of the address of said location second selected location corresponding to the second part of the address of the first selected location is the same as the second part of the address of the first selected location; and~~

~~(c) determining the address for said second selected location without transmitting said second part of the address of said second selected location by joining~~

~~the second part of the address of the first selected location with said first part of the address of said second location on the condition that said second part of the address of said second selected location is the same as the said second part of the address of the first selected location as determined in step (b).~~

2. (currently amended) The method of claim 1, further comprising storing the second part of the address of the first ~~selected~~ location in a register ~~in the memory~~.

3. (currently amended) The method of claim 1 ~~2~~, further comprising forming, if the second part of the address of the first location is substantially equivalent to the second part of the address of the second location, the address for the second location from the second part of the address of the first location and the at least one first part of the address of the second location. ~~providing an Address Enable signal that is active during at least part of step (a), wherein step (b) includes determining whether said Address Enable signal is inactive.~~

4. (currently amended) The method of claim 1, further comprising, if the second part of the address of the first location is not substantially equivalent to the second part of the address of the second location, transmitting on the bus a second part of the address of the second location, and forming the address of the second location from the at least one first part of the address of the second location and the second part of the address of the second location. ~~wherein said first and second parts of the address of the first and said second selected location are of equal size.~~

5. (currently amended) The method of claim 1 ~~2~~, wherein the transmission on the bus of the first location in the memory space comprises:

transmitting an address of a first register in a first address cycle, and storing the at least one first part of the address of the first location in the first register in a second address cycle;

transmitting an address of a second register in a third address cycle, and storing the second part of the address of the first location in the second register in

a fourth address cycle. ~~said first and second parts of the address of the first and said second selected location are of equal size.~~

6. (currently amended) The method of claim 1 ~~3~~, wherein the transmission on the bus of the first location in the memory space comprises:

transmitting an address of a first register in a first address cycle, and storing at least one first part of an address of a third location in the memory space in a first register in a second address cycle;

transmitting an address of a second register in a third address cycle, and storing the second part of the address of the third location in the second register in a fourth address cycle;

storing the at least one first part of the address of the first location in the first register in a fifth address cycle; and

storing the second part of the address of the first location in the second register in a sixth address cycle. ~~said first and second parts of the address of the first and said second selected location are of equal size.~~

7. (currently amended) An apparatus comprising: ~~for high speed addressing of a memory locations within the same page by accessing a first selected location in the memory space using at least a first and a second part of the address of the selected location, the apparatus comprising a logic circuit adapted to perform a method comprising the steps of:~~

a bus; ~~(a) transmitting a first part of the address of a second selected location in the memory space;~~

first and second registers coupled with the bus; and ~~(b) determining whether at least a second part of the address of said second selected location corresponding to the second part of the address of the first selected location is the same as the second part of the address of the first selected location; and~~

a unit, coupled with the bus and the first and second registers, that: ~~(c) determining the address for said second selected location without transmitting said second part of the address of said second selected location by joining the second part of the address of the first selected location with said first part of the address of said second location on the condition that said second part of the address of said second selected location is the same as the said second part of the address of the first selected location as determined in step (b).~~

selects the first register, in response to a transmission on the bus of an address of the first register, as a location to store first data, and stores the first data in the first register, in response to transmission of the first data on the bus in a next data cycle, the first data being at least one first part of an address of a first location in a memory space;

selects the second register, in response to a transmission on the bus of an address of the second register, as a location to store second data, and stores the second data in the second register, in response to a transmission of the second data on the bus in a next data cycle, the second data being a second part of the address of the first location in the memory space;

determines that a first condition is true, the first condition being that the first register is selected as a location to store first data and the second register is selected as a location to store second data; and

stores third data in the first register, in response to transmission of third data on the bus, if the first condition is true, the third data being at least one first part of an address of a second location in the memory space.

8. (currently amended) The apparatus of claim 7, wherein the unit stores fourth data in the second register, in response to transmission of the fourth data on the bus, if the first

condition is true, the fourth data being a second part of the address of the second location in the memory space. ~~adapted to store the second part of the address of the first selected location in a register in the memory.~~

9. (currently amended) The apparatus of claim 7~~-8~~, wherein the unit:

determines that a second condition is true, the second condition being that at least one first part of an address of the second location in the memory space has been transmitted on the bus in a particular address cycle;

determines that a third condition is true, the third condition being that a first control signal associated with the bus indicates that a next bus cycle following the particular address cycle is not an address cycle; and

determines, if the first, second, and third conditions are true, that the second part of the address of the first location is substantially equivalent to a second part of the address of the second location. ~~said logic circuit is further adapted to receive an Address Enable signal that is active during at least part of step (a), wherein said logic circuit is further adapted so that step (b) includes determining whether said Address Enable signal is inactive.~~

10. (currently amended) The apparatus of claim 9~~-7~~, wherein the unit, if the second part of the address of the first location is substantially equivalent to the second part of the address of the second location, forms the address for the second location from the second part of the address of the first location and the at least one first part of the address of the second location. ~~adapted so that said first and second parts of the address of the first and said second selected location are of equal size.~~

11. (currently amended) The apparatus of claim 10~~,-8~~ wherein the unit, if the second part of the address of the first location is not substantially equivalent to the second part of the address of the second location, forms the address for the second location from the at least one first part of the address of the second location and the second part of the address of second location. ~~adapted so that said first and second parts of the address of the first and said second selected location are of equal size.~~

12. (currently amended) The apparatus of claim 11, ~~9~~ further comprising a machine readable medium embodying a program of instructions for execution by the unit, the instructions to determine whether the first, second, and third conditions are true, and to form the address for the second location in the memory space. ~~adapted so that said first and second parts of the address of the first and said second selected location are of equal size.~~

13. (currently amended) A system comprising: ~~A machine readable medium embodying a program of instructions for execution by a machine to perform a method for high speed addressing of memory within the same page by accessing a first selected location in the memory space using at least a first and a second part of the address of the selected location, the method comprising the steps of:~~

a bus; ~~(a) transmitting a first part of the address of a second selected location in the memory space;~~

first and second registers coupled with the bus; ~~(b) determining whether at least a second part of the address of said second selected location corresponding to the second part of the address of the first selected location is the same as the second part of the address of the first selected location; and~~

a unit, coupled with the bus and the first and second registers, that: ~~(c) determining the address for said second selected location without transmitting said second part of the address of said second selected location by joining the second part of the address of the first selected location with said first part of the address of said second location on the condition that said second part of the address of said second selected location is the same as the said second part of the address of the first selected location as determined in step (b).~~

determines that a first condition is true, the first condition being that an address of a first location in a memory space has been stored in the first and second registers, the address of the first location including at least one first part and a second part;

determines that a second condition is true, the second condition being that at least one first part of an address of a second location in the memory space has been transmitted on the bus in a particular address cycle;

determines that a third condition is true, the third condition being that a first control signal associated with the bus indicates that a next bus cycle following the particular address cycle is not an address cycle; and

determines, if the first, second, and third conditions are true, that the second part of the address of the first location is substantially equivalent to a second part of the address of the second location.

14. (currently amended) The system of claim 13, wherein the unit forms, if the second part of the address of the first location and the second part of the address of the second location are substantially equivalent, the address for the second location from the at least one first part of the address of the second location and the second part of the address of the first location. ~~The machine readable medium of claim 13 adapted so that the method further comprising storing the second part of the address of the first selected location in a register in the memory.~~

15. (currently amended) The system of claim 14, wherein the unit forms, if the second part of the address of the first location and the second part of the address of the second location are not substantially equivalent, the address for the second location from the at least one first part of the address of the second location and the second part of the address of the second location. ~~The machine readable medium of claim 14 adapted so that the method further comprises providing an Address Enable signal that is active during at least part of step (a), wherein step (b) includes determining whether said Address Enable signal is inactive.~~

16. (currently amended) The system of claim 15, further comprising a processor, wherein the processor determines that the second part of the address of the first location is substantially equivalent to a second part of the address of the second location. ~~The~~

~~machine readable medium of claim 13 adapted so that said first and second parts of the address of the first and said second selected location are of equal size.~~

17. (currently amended) The system of claim 16, further comprising a processor, coupled with the bus, wherein the processor provides the first control signal. ~~The machine readable medium of claim 14 adapted so that said first and second parts of the address of the first and said second selected location are of equal size.~~

18. (currently amended) The system of claim 13, further comprising a memory having a plurality of locations, each location having an address in the memory space. ~~The machine readable medium of claim 15 adapted so that said first and second parts of the address of the first and said second selected location are of equal size.~~

19. (currently amended) The method of claim 3, further comprising providing a machine readable medium embodying a program of instructions for execution by a machine to perform determination if the first, second, and third conditions are true, and to form the address for the second location in the memory space. ~~The machine readable medium of claim 16 adapted so that said first and second parts of the address of the first and second selected locations are each 8 bits.~~

20. (currently amended) The apparatus of claim 7, further comprising a memory, the memory having a plurality of locations, each location having an address in the memory space. ~~The machine readable medium of claim 18 adapted so that said first and second parts of the address of the first and second selected locations are each 8 bits.~~